first and second regions in said epitaxial layer each having a second conductivity type opposite the first conductivity type, said first and second regions extending from a surface of said epitaxial layer opposite said substrate into said epitaxial layer to form respective first and a second junctions therewith; and

an isolating element positioned between said first and said second regions and extending from the surface of said epitaxial layer at least as far as a top surface of said substrate, said isolating element having a length substantially equal to a width of the semiconductor chip and dividing the semiconductor chip into two portions each respectively including said first and said second regions, said isolating element also terminating above a bottom surface of said substrate.

REMARKS

The Examiner is thanked for his thorough examination of the present application. Claims 12, 17, and 22 have been amended to more clearly define the subject matter thereof over the prior art. Support for the amendments may be found on page 8, lines 24-26 of the originally filed specification and in FIGS. 1, 3a-3d, for example. Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached pages are captioned "**Version with Markings to Show Changes Made**."

In view of the amendments and the supporting arguments presented in detail below, it is submitted that all of the claims are patentable.

I. The Claimed Invention

The present invention is directed to an integrated structure. As recited in amended independent Claim 17, for

example, the integrated structure includes a substrate having a first conductivity type and an epitaxial layer on the substrate. The epitaxial layer has the first conductivity type and a conductivity less than a conductivity of the substrate. Moreover, the integrated structure also includes first and second regions in the epitaxial layer each having a second conductivity type opposite the first conductivity type. The first and second regions extend from a surface of the epitaxial layer opposite the substrate into the epitaxial layer to form respective first and a second junctions therewith. Further, the integrated structure also includes an isolating element positioned between the first and the second regions and extending from the surface of the epitaxial layer at least as far as a top surface of the substrate. The isolating element partially surrounds at least one of the first and second regions. Furthermore, the isolating element also terminates above a bottom surface of the substrate.

Independent Claims 12 and 22 are directed to related integrated structures and have similarly been amended to recite that the isolating elements thereof terminate above a lower surface of the substrate. Because of the isolating element and relative conductivities of the various elements recited in these claims, an injection of current through the epitaxial layer from the first to the second region is advantageously reduced when the first junction is directly biased, for example.

II. The Claims Are Patentable

The Examiner rejected independent Claims 12, 17, and 22 over Chang et al. This patent discloses an integrated circuit chip which has full trench dielectric isolation of each portion of the chip. Initially the chip substrate **10** is of conventional thickness (e.g., 500 um) and has semiconductor

devices formed therein. After etching trenches **72** in the substrate **10** and filling them with dielectric material (see FIGS. 2 and 3 of Chang et al.), a heat sink cap **100** is attached to the passivation layer **96** on the substrate **10** front side surface. The substrate backside surface is removed (by grinding or chemical mechanical polishing (CMP)) to expose the bottom portion of the trenches **72** (see FIGS. 7 of Chang et al). Thus, the dielectric isolation material in the trenches extends completely through the substrate **10**. This is done to fully isolate each portion of the die and eliminate mechanical stresses at the trench **72** bottoms. Thereafter, drain or collector electrical contacts **104a**, **104b** are provided on the substrate **10** backside surface.

In contrast to the integrated circuit chip of Chang et al., the isolating element recited in each of the above noted amended independent claims terminates above the bottom surface of the substrate. That is, the present invention achieves desired isolation based upon the isolation element and the relative conductivities of the various elements (see, e.g., page 9 of the originally filed specification). However, Chang et al. requires that the dielectric material extend completely through the substrate to achieve the desired isolation properties. To do so, the substrate thereof has to be reduced in thickness from 500 µm to about 5 to 100 µm via CMP, etc. (see col. 6, lines 5-24 of Chang et al.), a costly and time consuming procedure. Yet, the integrated structure of the present invention provides desired isolation without such additional processing.

As such, Chang et al. fails to teach or fairly suggest all of the elements recited in each of the above noted independent claims, and the rejection of these claims based upon Chang et al. must therefore be withdrawn. Moreover, for the reasons set forth above, Cheng et al. in fact would have

taught those of skill in the art away from making an integrated structure with dielectric-filled trenches that terminate above the bottom surface of the substrate. That is, Chang et al. teaches that such trenches must extend completely through the substrate to achieve "full electrical isolation," as is the stated purpose of the patent (see col. 7, lines 19-21). To have done otherwise would therefore have also rendered Chang et al. unsatisfactory for this intended purpose.

Accordingly, it is submitted that independent Claims 12, 17, and 22 are patentable over the prior art. Their respective dependent claims, which recite yet further distinguishing features, are also patentable over the prior art and require no further discussion herein.

CONCLUSIONS

In view of the amendments to the claims and the arguments presented above, it is submitted that all of the claims are patentable. Accordingly, a Notice of Allowance is respectfully requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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In re Patent Application of:
ERRATICO
Serial No. **09/899,573**
Filing Date: **July 5, 2001**
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 12, 17, and 22 have been amended as follows:

12. (Amended) An integrated structure comprising:

a substrate having a first conductivity type;

an epitaxial layer on said substrate and having the first conductivity type and a conductivity less than a conductivity of said substrate;

first and second regions in said epitaxial layer each having a second conductivity type opposite the first conductivity type, said first and second regions extending from a surface of said epitaxial layer opposite said substrate into said epitaxial layer to form respective first and a second junctions therewith; and

an isolating element positioned between said first and said second regions and extending from the surface of said epitaxial layer at least as far as a top surface of said substrate for reducing an injection of current through said epitaxial layer from said first region to said second region when the first junction is directly biased, said isolating element comprising a dielectric material adjacent said epitaxial layer and polycrystalline silicon spaced apart from said epitaxial layer by said dielectric material, said isolating element also terminating above a bottom surface of said substrate.

17. (Amended) An integrated structure comprising:

a substrate having a first conductivity type;

an epitaxial layer on said substrate and having the first conductivity type and a conductivity less than a conductivity of said substrate;

first and second regions in said epitaxial layer each having a second conductivity type opposite the first conductivity type, said first and second regions extending from a surface of said epitaxial layer opposite said substrate into said epitaxial layer to form respective first and a second junctions therewith; and

an isolating element positioned between said first and said second regions and extending from the surface of said epitaxial layer at least as far as a top surface of said substrate, said isolating element partially surrounding at least one of said first and second regions, said isolating element also terminating above a bottom surface of said substrate.

22. (Amended) An integrated structure formed on a semiconductor chip and comprising:

a substrate having a first conductivity type;

an epitaxial layer on said substrate and having the first conductivity type and a conductivity less than a conductivity of said substrate;

first and second regions in said epitaxial layer each having a second conductivity type opposite the first conductivity type, said first and second regions extending from a surface of said epitaxial layer opposite said substrate into said epitaxial layer to form respective first and a second junctions therewith; and

an isolating element positioned between said first and said second regions and extending from the surface of said epitaxial layer at least as far as a top surface of said substrate, said isolating element having a length substantially equal to a width of the semiconductor chip and dividing the semiconductor chip into two portions each respectively including said first and said second regions,

said isolating element also terminating above a bottom surface of said substrate.

In re Patent Application of:
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: DIRECTOR, U.S. PATENT AND TRADEMARK OFFICE, WASHINGTON, D.C. 20231, on this 22nd day of August, 2002.